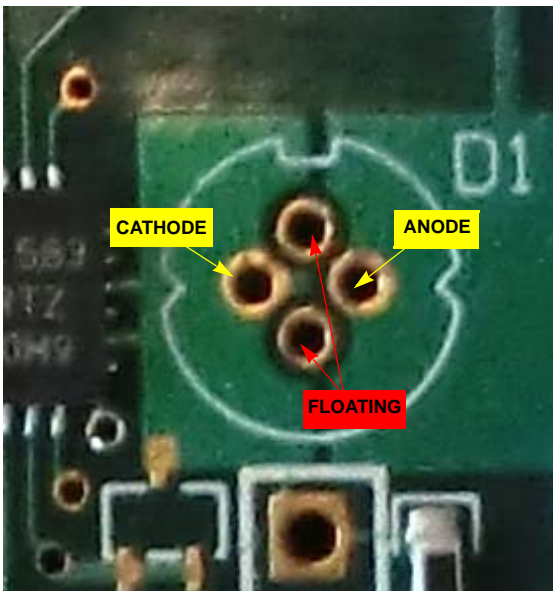


# Attaching Loads to a High Current LDD Evaluation Board

The ISL58303HC-EVALZ provides a compact, low inductance evaluation board that accommodates either a passive or Laser load. The board was designed around a floating laser with a footprint that allows a laser to easily be attached either to the top or the bottom of the board.

## Attaching Floating Lasers

The anode via is connected to the power supply post labeled Viaser. The cathode via is connected to the 58303 device output pins CH1, CH2 and CH3. These output pins are shorted together with the cathode board trace.

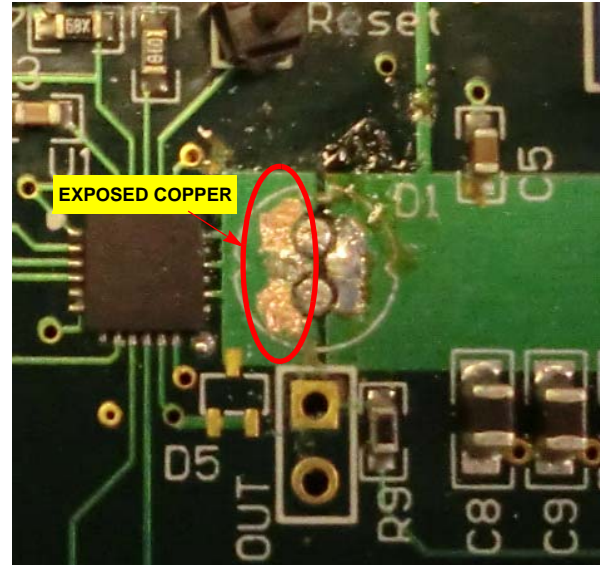


**FIGURE 1. 58303HC-EVALZ LASER FOOTPRINT**

Pin 2 is a no connected on floating lasers and can be connected to either of the two floating vias. One for lasers configured on the top of the board and the other if the laser is on the bottom.

## Dual Cathode Lasers

Dual cathode lasers can also be attached to this board on either the top or the bottom side of the board. When attaching this type of laser the anode pin is connected to the anode via but the cathode pins are attached through the floating vias. For this to work electrically the floating vias must be shorted to cathode via and trace. The first step is to remove the solder mask from the cathode trace in the area surrounding the floating vias. Removal of the solder mask can easily be done lightly scraping it away with an Exacto knife. Care should be taken not to remove excessive amounts of the copper beneath. This is shown in Figure 2.



**FIGURE 2. CATHODE SOLDER MASK REMOVED**

Once the solder mask is removed apply solder flux to the exposed copper and apply a large mound of solder. Insert the laser into position soldering it's pins to all 3 vias. The last step is to bridge solder from the cathode trace to the floating vias now attached to the laser cathode pins. Care must be taken so that the solder does not bridge to the anode pin or trace. Soldering the laser to the bottom side of the board is the preferred configuration. It allows the laser body to be flush with the board resulting in the lowest inductance and the most accurate performance measurements. The laser can be attached to the top side of the board but the disadvantage is that it must stand up about 5mm to allow access for soldering to the floating vias. The increased height increases the lead length which increases the parasitic inductance. This inductance will increase the laser rise and fall times. Figure 3 shows a bottom side laser attachment.

A dual anode laser would be addressed in a similar fashion. The difference is that the floating pins would be shorted to the anode trace instead of the cathode.

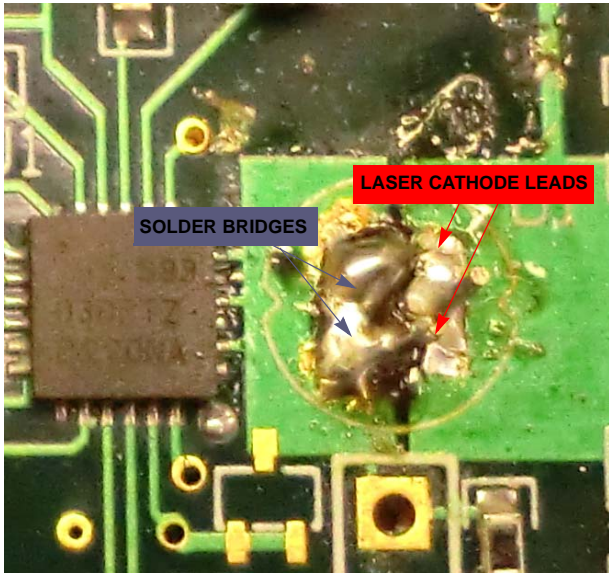


FIGURE 3. DUAL CATHODE LASER ATTACHED

For total output currents above 2A the load resistance should total  $0.5\Omega$ . For currents less than 2A  $1.0\Omega$  total resistance is a good value. The Target is to have a 1V to 2V drop/swing across the load. This gives a good oscilloscope enough resolution to accurately measure rise/fall times. Figure 5 shows 4 x  $4\Omega$  resistors soldered to a board.

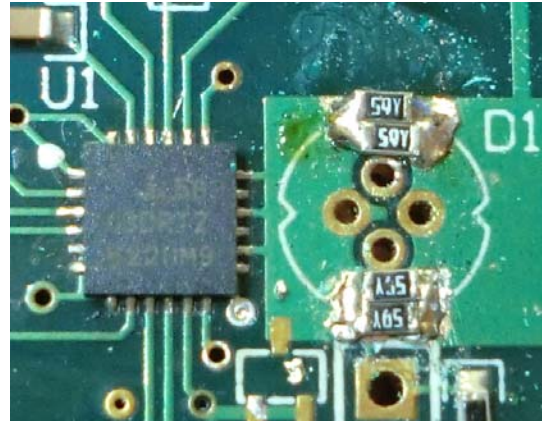


FIGURE 5. LOAD RESISTORS ATTACHED

## Resistor Loads

The best indicator of chip performance is a measurement of the voltage across a resistive load. Laser impedance has a large inductive component which has a large effect on measured rise and fall times. The procedure for attaching resistor loads is similar to attaching a dual cathode laser. The solder mask is carefully scraped away and resistors are attached bridging the power supply and chip output traces. It is best to connect 3 or 4 resistors in parallel to lower the total parasitic inductance due to the resistor ESL. Figure 4 shows a board with the solder mask scraped away allowing resistor attaching.

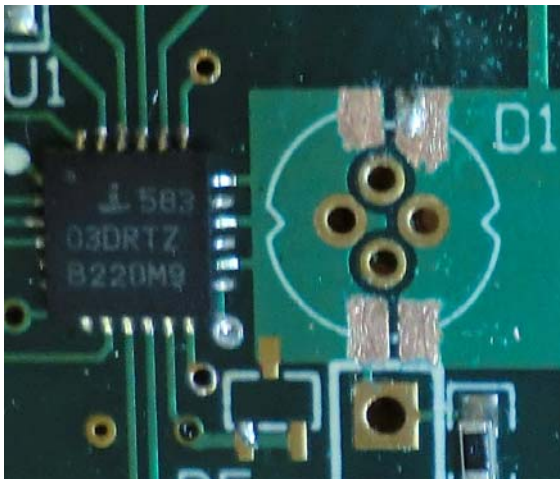


FIGURE 4. SOLDER MASK REMOVED FOR RESISTORS

## Additional Questions

Stephen M. Wickland

Optical System Solutions

[swicklan@intersil.com](mailto:swicklan@intersil.com)

Intersil Corporation reserves the right to make changes in circuit design, software and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that the Application Note or Technical Brief is current before proceeding.

For information regarding Intersil Corporation and its products, see [www.intersil.com](http://www.intersil.com)